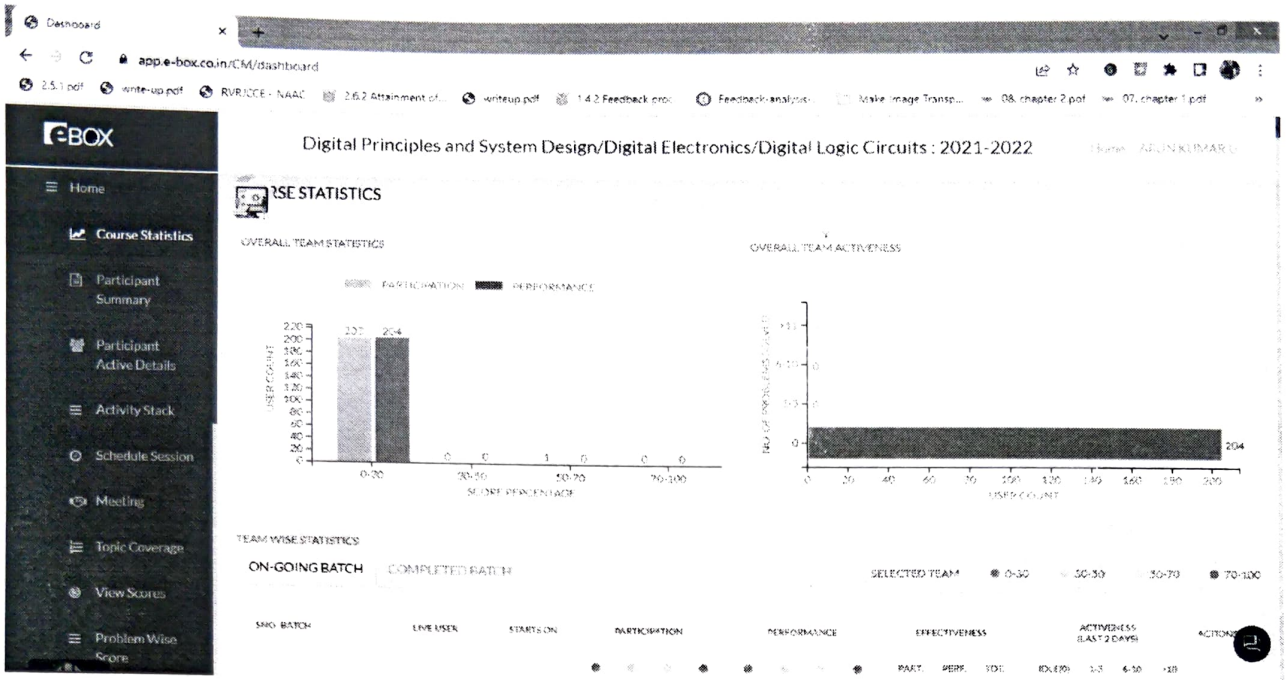
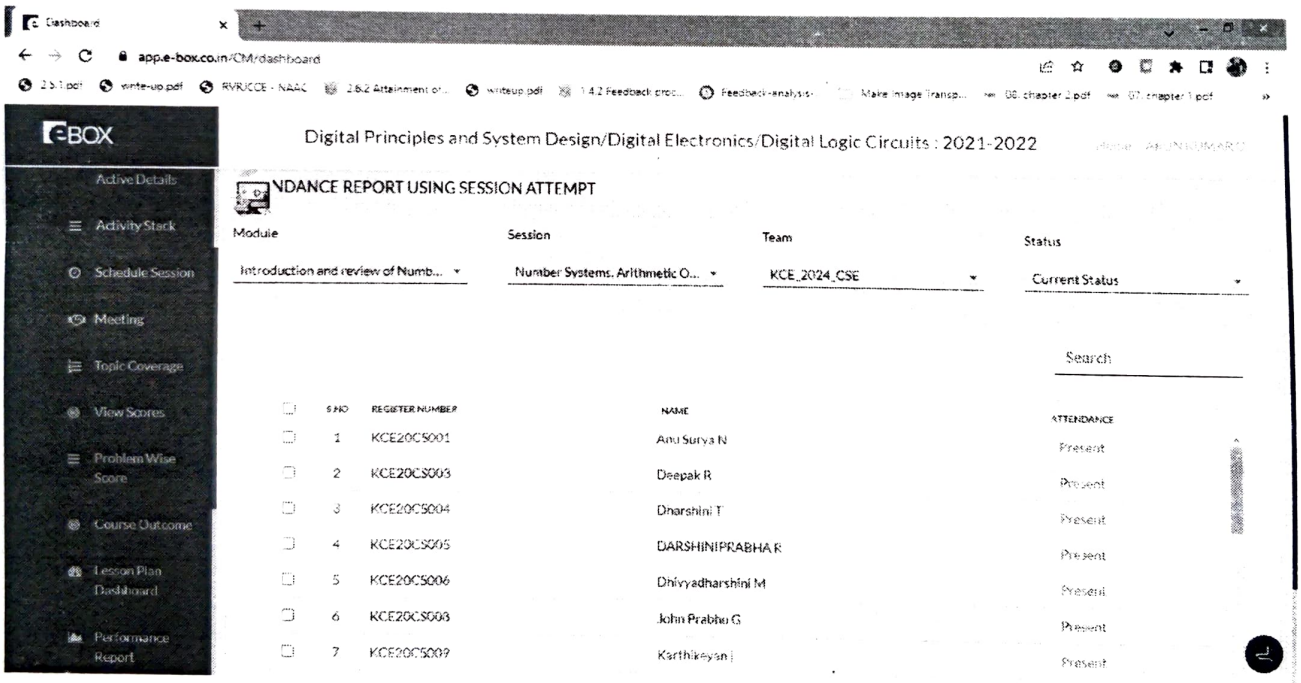
Examination –ScreenShot of Tech Enabled Assessment:





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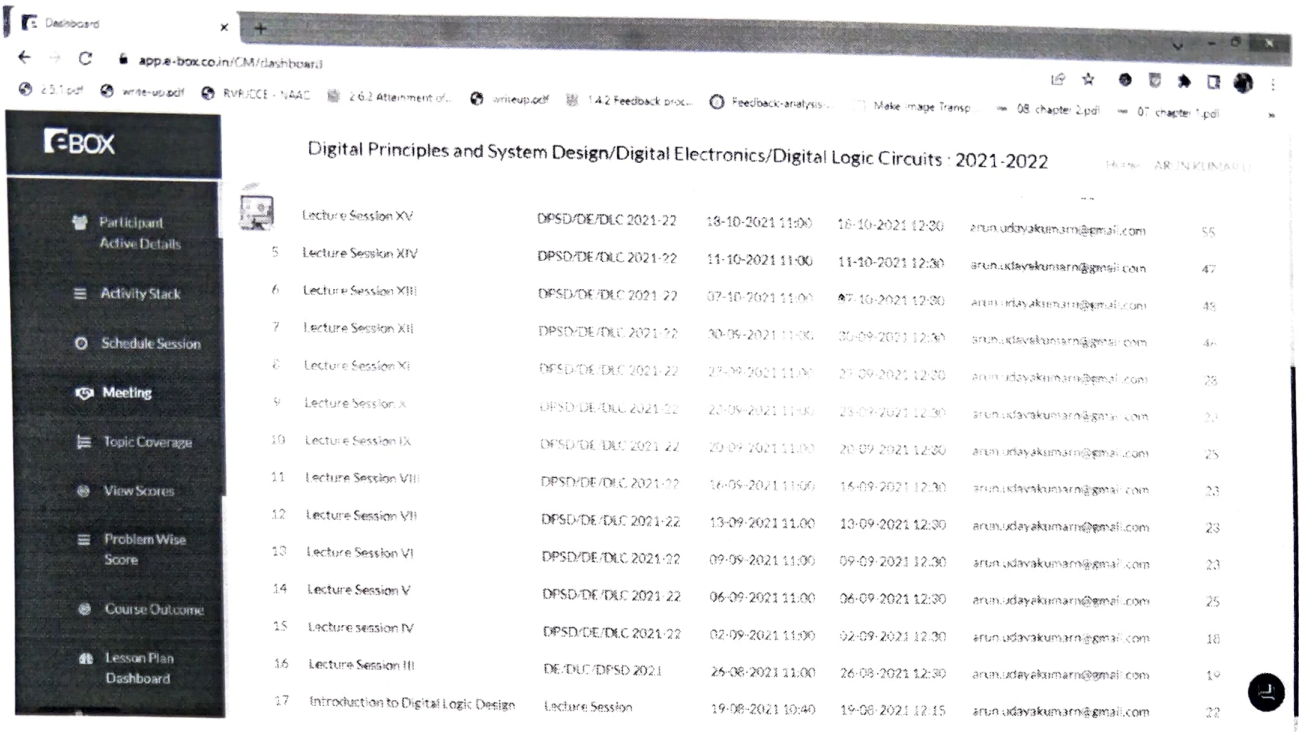

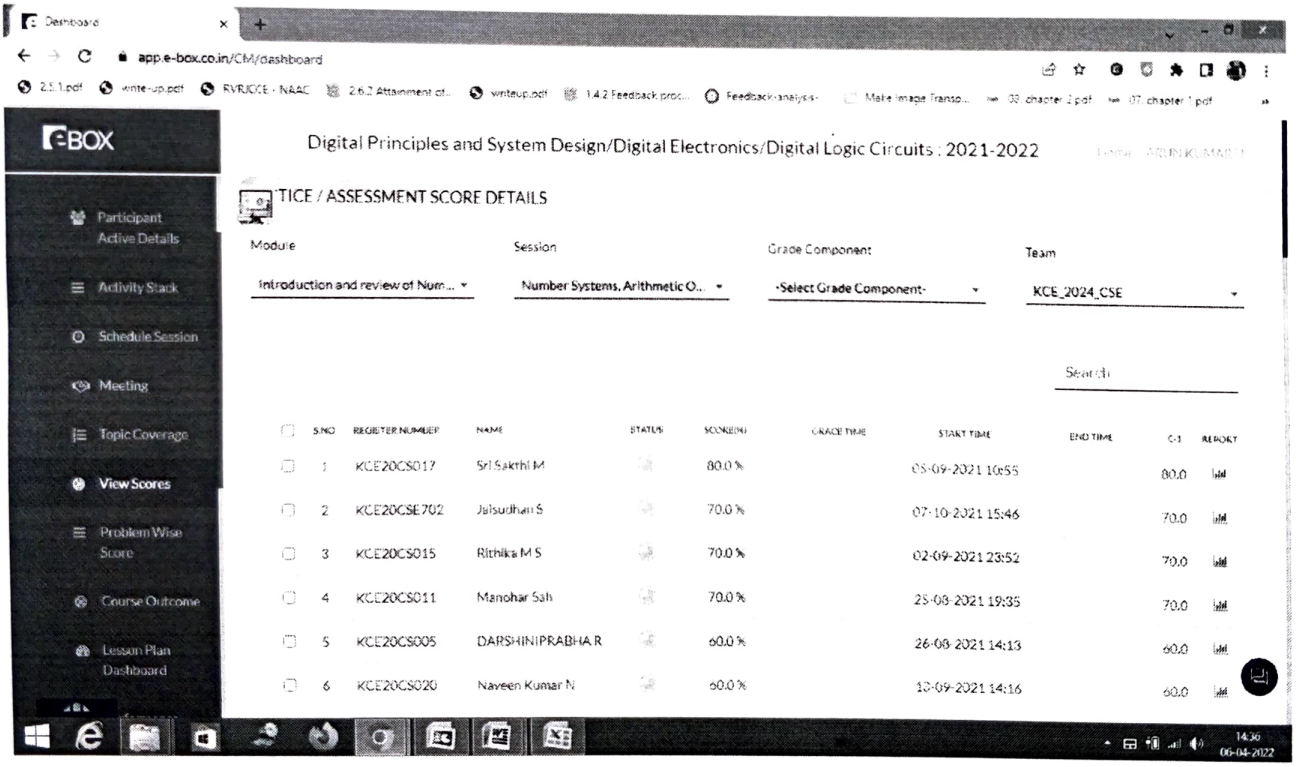

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Principal
Kathir College of Engineering,
"Wisdom Trees" Avinashi Road,
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Sri Sakthi M

KCE20CS017

Kathir College of Engineering

Outliers

1/28 BATCH RANK

71 TOTAL HOURS SPENT

7/53 TOPICS COMPLETED

0/56 SKILL PROBLEMS

3024/1398 KNOWLEDGE PROBLEMS

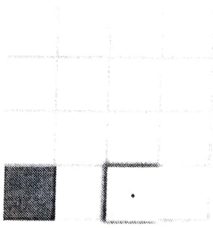
Participation

65%
Attended 178 of 199 Sessions

Performance

0%
Attended 2 of 54 Assessments

Quadrant Summary



QUADRANT 14

Low Calibre, Consistent Learner

OUTLIERS

SUITABILITY

You are qualified for job roles offering 3L+ Salary.

AIM FOR:

You can aim to become part of the Standard+ Group (4L+ salary)..

HOW TO IMPROVE YOUR METRICS?

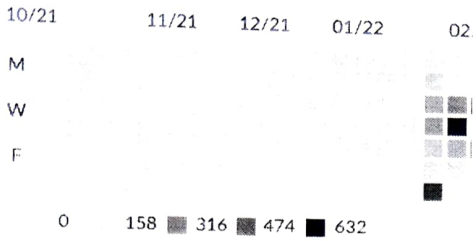
1) Have confidence in your abilities and avoid solving problems as a group.
2) Solve them individually. Attend all nugget assessments to improve your confidence level.
3) Rework on the topics/exercises in which you lack confidence by which your completion will improve.

Practice Session Score Details

SNO	TOPIC	I-LEARN	I-EXPLORE	I-ANALYSE	I-DESIGN
1	Introduction and review of Number systems, Arithmetic operations and Binary Codes	100.0% 2/2	80.0%	0.0%	AB
2	Boolean Algebra and Logic Gates - Theorems and Properties - I	100.0% 2/2	0.0%	AB	AB
3	Boolean Algebra and Logic Gates - Theorems and Properties - II	100.0% 2/2	0.0%	0.0%	AB
4	Boolean Functions - Canonical and Standard Forms - I	100.0% 2/2	0.0%	AB	AB
5	Boolean Functions - Canonical and Standard Forms - II	100.0% 2/2	20.0%	AB	AB
6	Simplification of Boolean Functions using Karnaugh Map - I	100.0% 2/2	80.0%	13.33%	68.75%
7	Simplification of Boolean Functions using Karnaugh Map - II	100.0% 2/2	100.0%	46.67%	81.25%
8	Simplification of Boolean Functions using Karnaugh Map - III	100.0% 2/2	100.0%	100.0%	80.42%
9	Simplification of Boolean Functions using Karnaugh Map -Example Problems - 1	100.0% 2/2	80.0%	100.0%	93.75%
10	Simplification of Boolean Functions using Karnaugh Map - Example Problems - 2	100.0%	100.0%	80.0%	75.0%
11	NAND and NOR Implementation	100.0% 2/2	100.0%	100.0%	66.67%
12	NAND and NOR Implementation - Example Problems	100.0%	100.0%	100.0%	50.0%
13	Combinational Circuits –Analysis and Design Procedures	100.0%	20.0%	AB	AB
14	Combinational Circuit Design - Example Problems - 1	100.0%	100.0%	50.0%	12.5%
15	Combinational Circuit Design - Example Problems - 2	100.0%	75.0%	50.0%	25.0%

16	Binary Adder-Subtractor -Decimal Adder-Binary Multiplier	100.0%	0.0%	0.0%	AB
17	Magnitude Comparator-Code converter	100.0%	100.0%	No Session	31.25%
18	Code Converters - Example Problems	100.0%	No Session	25.0%	[illegible]
19	Decoder and Encoder	100.0%	100.0%	80.0%	[illegible]
20	Multiplexer and Demultiplexer	80.0%	100.0%	100.0%	[illegible]
21	MUX and DeMUX - Example Problems	100.0%	100.0%	100.0%	No Session
22	Logical Circuit Design - Example Problems	100.0%	100.0%	100.0%	[illegible]
23	Introduction to HDL and HDL Models of Combinational circuits	AB	AB	AB	AB
24	Combinational and Logical Circuit Design - Example Programs	0.0%	0.0%	0.0%	0.0%
25	Sequential Circuits - SR,JK, T and D Flipflops and Latches, Types of Triggering	100.0%	2.38%	[illegible]	0.0%
26	Analysis of Clocked Sequential Circuits	100.0%	0.0%	100.0%	0.0%
27	Flipflops, Sequential Circuit Analysis and Design - Example Problems - 1	100.0%	100.0%	100.0%	12.5%
28	Sequential Circuit Analysis and Design - Example Problems - 2	100.0%	100.0%	100.0%	No Session
29	State diagram, Reduction and Assignment	100.0%	100.0%	100.0%	No Session
30	State Reduction and Assignment - Example Problems	100.0%	100.0%	100.0%	No Session
31	Synchronous and Asynchronous Counters - Design Procedure	100.0%	[illegible]	100.0%	25.0%
32	Synchronous and Asynchronous Counters - Example Problems and Shift Registers	100.0%	[illegible]	100.0%	15.0%
33	Counters - Example Problems - 1	100.0%	20.0%	100.0%	23.33%
34	Counters and Shift Registers - Example Problems - 2	100.0%	20.0%	100.0%	8.33%
35	HDL Models of Sequential circuits	100.0%	100.0%	No Session	0.0%
36	Sequential Circuit Design - Example Programs	100.0%	100.0%	No Session	0.0%
37	Asynchronous sequential logic circuits-Transition stability, flow stability, PFT	100.0%	100.0%	[illegible]	12.5% 2 / 2
38	Analysis of asynchronous sequential logic circuits - I	100.0%	100.0%	[illegible]	25.0%
39	Analysis of asynchronous sequential logic circuits - II	100.0%	100.0%	No Session	12.5%
40	Asynchronous sequential Circuit Analysis and Design - Example Problems - 1	100.0%	100.0%	No Session	16.67%
41	Flow diagram and Table - Reduction and Assignment	100.0%	100.0%	25.0%	0.0%
42	Flow diagram and Table - Reduction and Assignment - Example Problems	100.0%	100.0%	No Session	72.73%
43	Races, Cycles and Hazards	100.0%	100.0%	100.0%	No Session
44	Races, Cycles and Hazards - Example Problems	100.0%	100.0%	100.0%	No Session
45	RAM –Memory Decoding	100.0%	100.0%	[illegible]	95.19%
46	Error Detection and Correction -ROM	100.0%	100.0%	82.5%	100.0%
47	Programmable Logic Array	100.0%	[illegible]	0.0%	0.0%
48	Programmable Array Logic	100.0%	100.0%	No Session	100.0%
49	Digital Logic Families	100.0%	100.0%	100.0%	100.0%
50	Test	AB 0 / 2	AB	AB	AB 0 / 2

Problem Solved Metrics



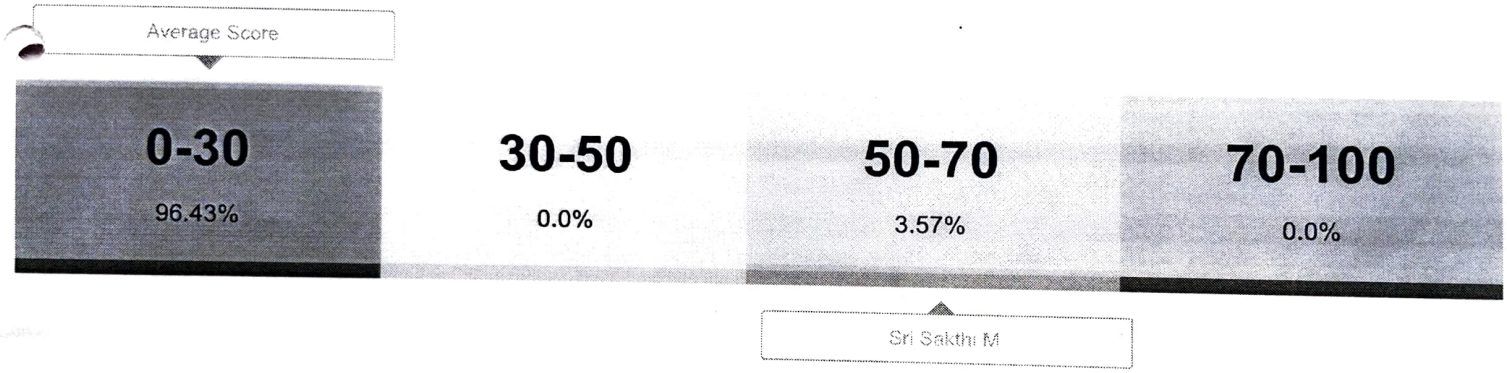
Time Spent Metrics

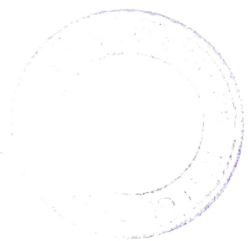
Total Hour Spent:	71 Hrs
Total Day Spent:	34 Days
Average Time Spent:	2 Hrs

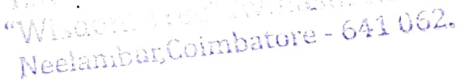
Assessment Score Details

SNO	TOPIC	SESSION	ASSESSMENT DATE	SCORE
1	Error Detection and Correction -ROM	Error Detection and Correction -ROM	16-02-2022 03:02 PM	0.0
2	Programmable Array Logic	Programmable Array Logic	24-02-2022 11:02 AM	0.0

User Score Status







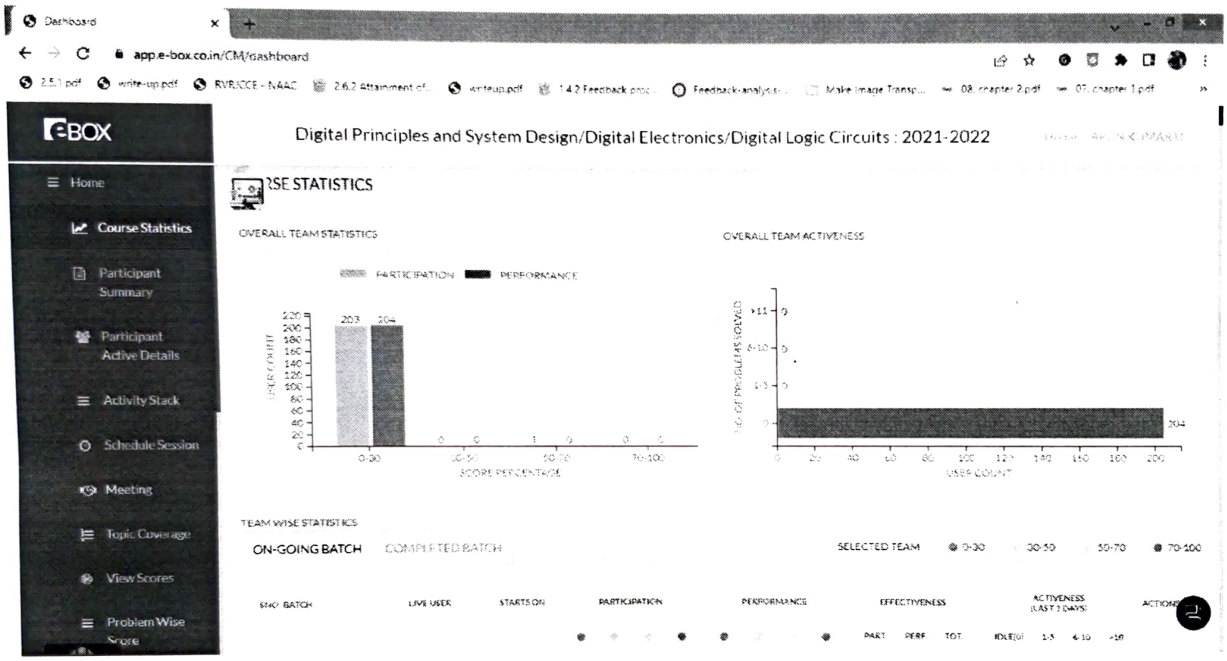
Kathir College of Engineering

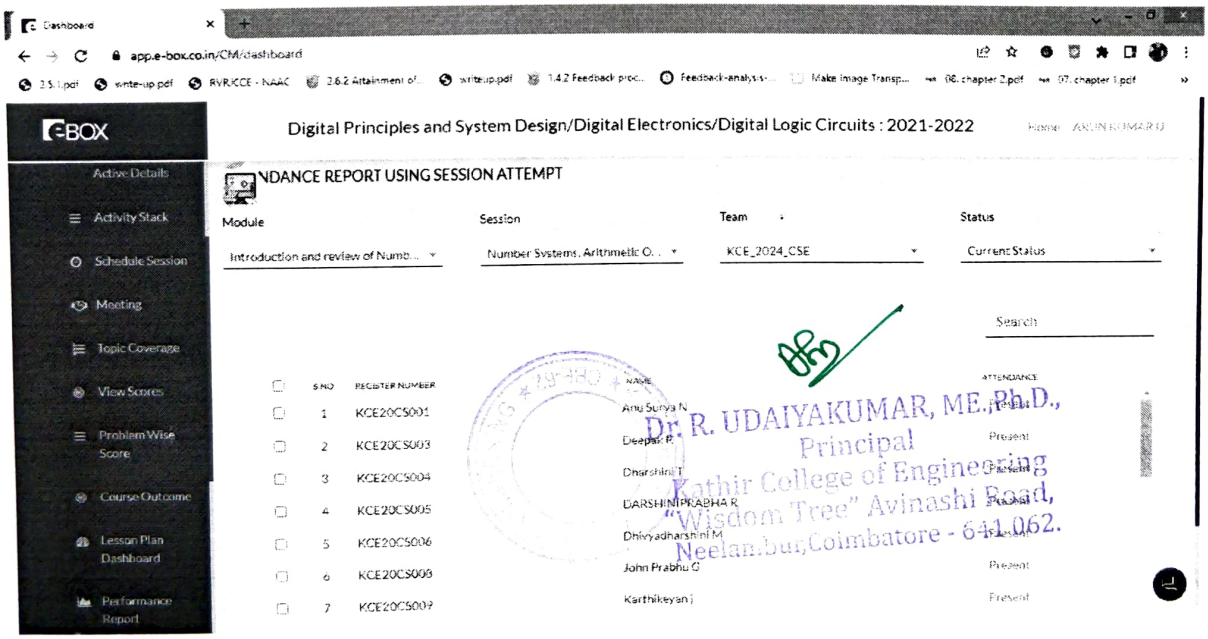
[Approved by AICTE | Affiliated to Anna University | Accredited by NAAC]

Wisdom Tree, Neelambur, Avinashi Road, Coimbatore-62

Activities Implemented Based on Strategic Planning

Following Effective Teaching – Learning Process (Tech Enabled Teaching and Learning)





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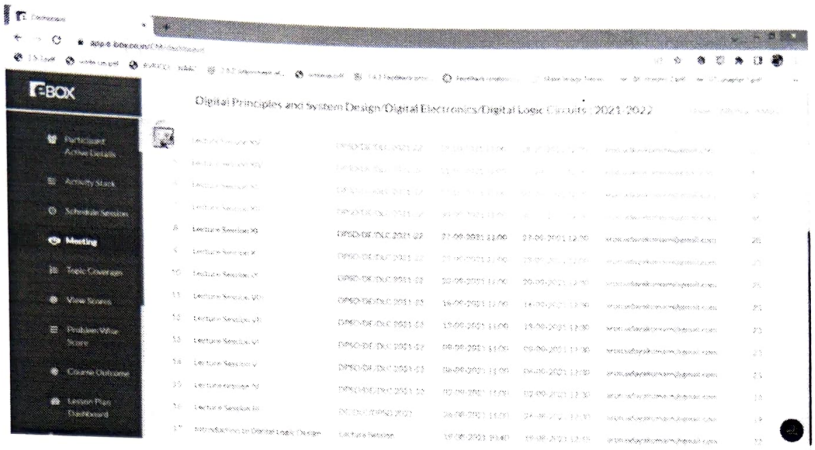

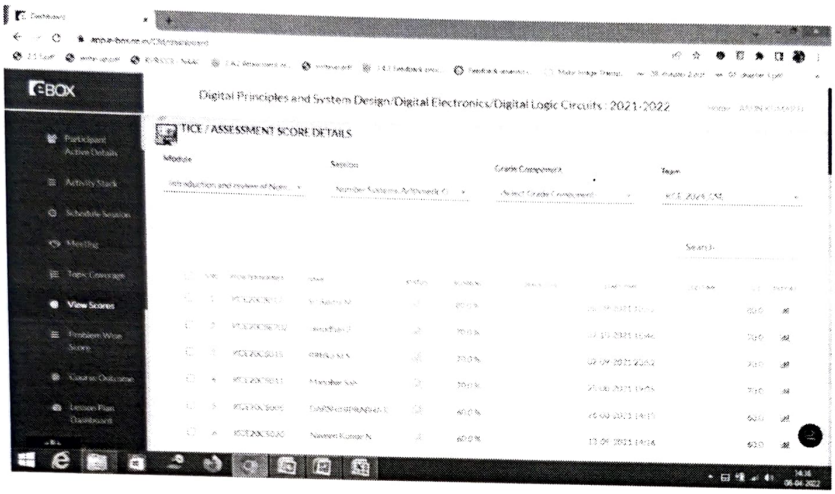

Following Effective Teaching – Learning Process (Smart Board Usage)

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Principal
Kathir College of Engineeri
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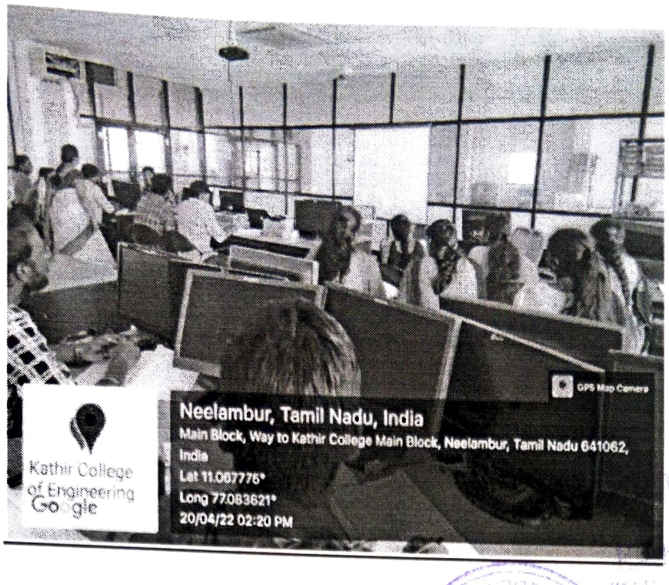
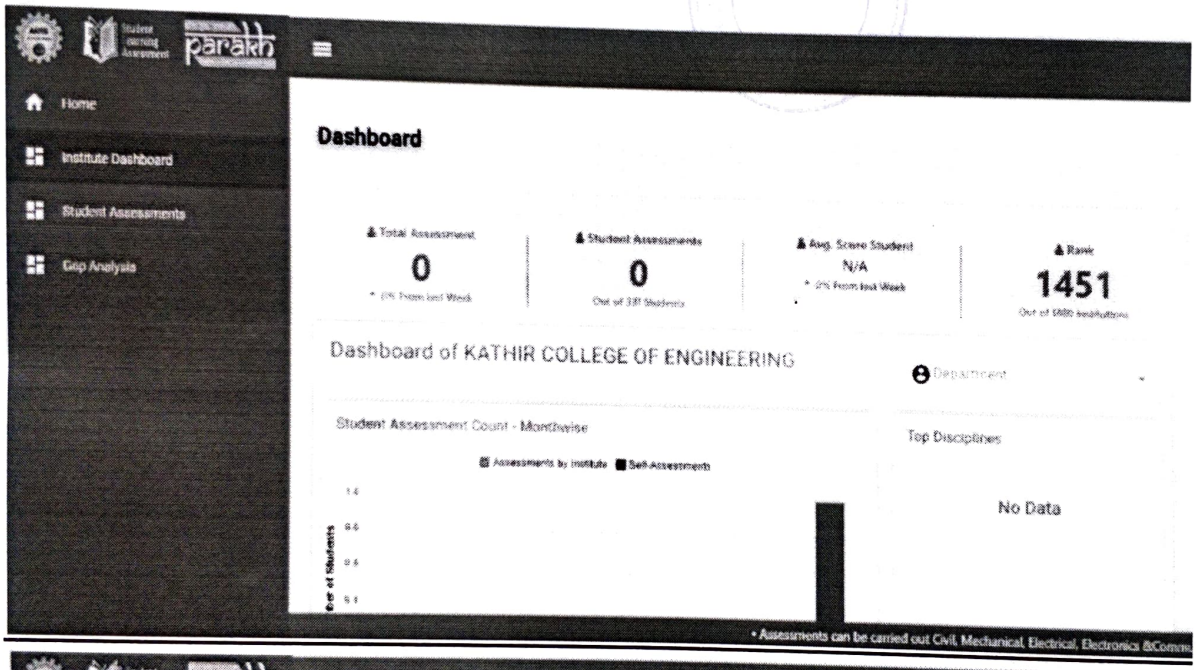
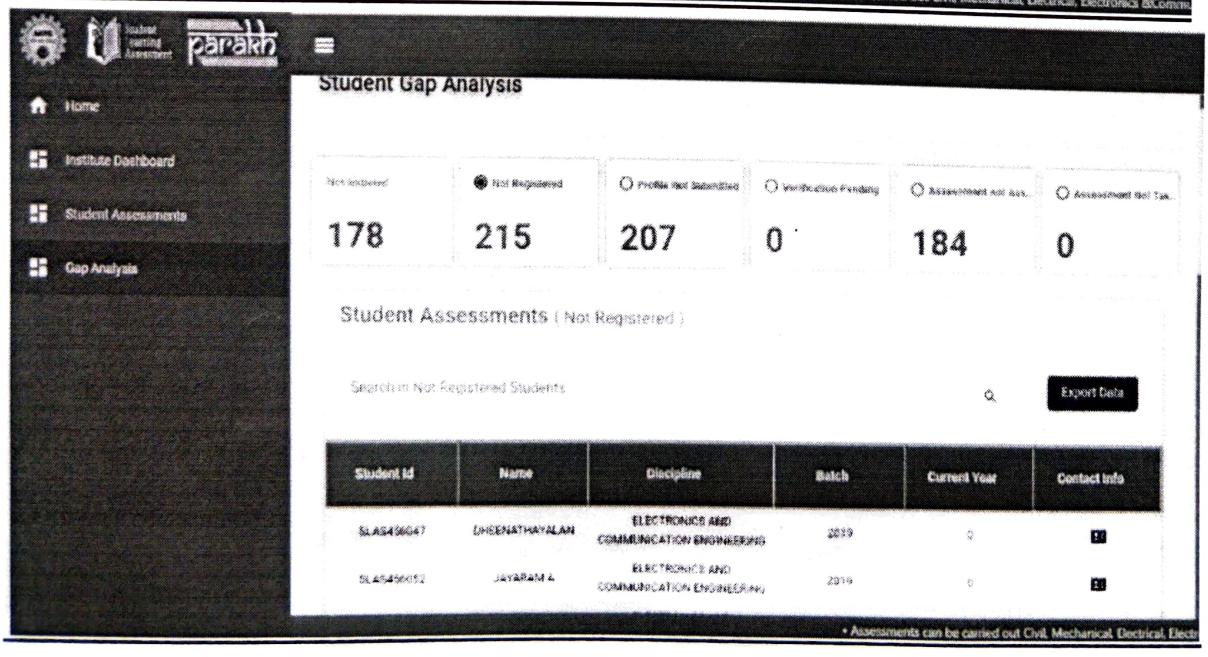
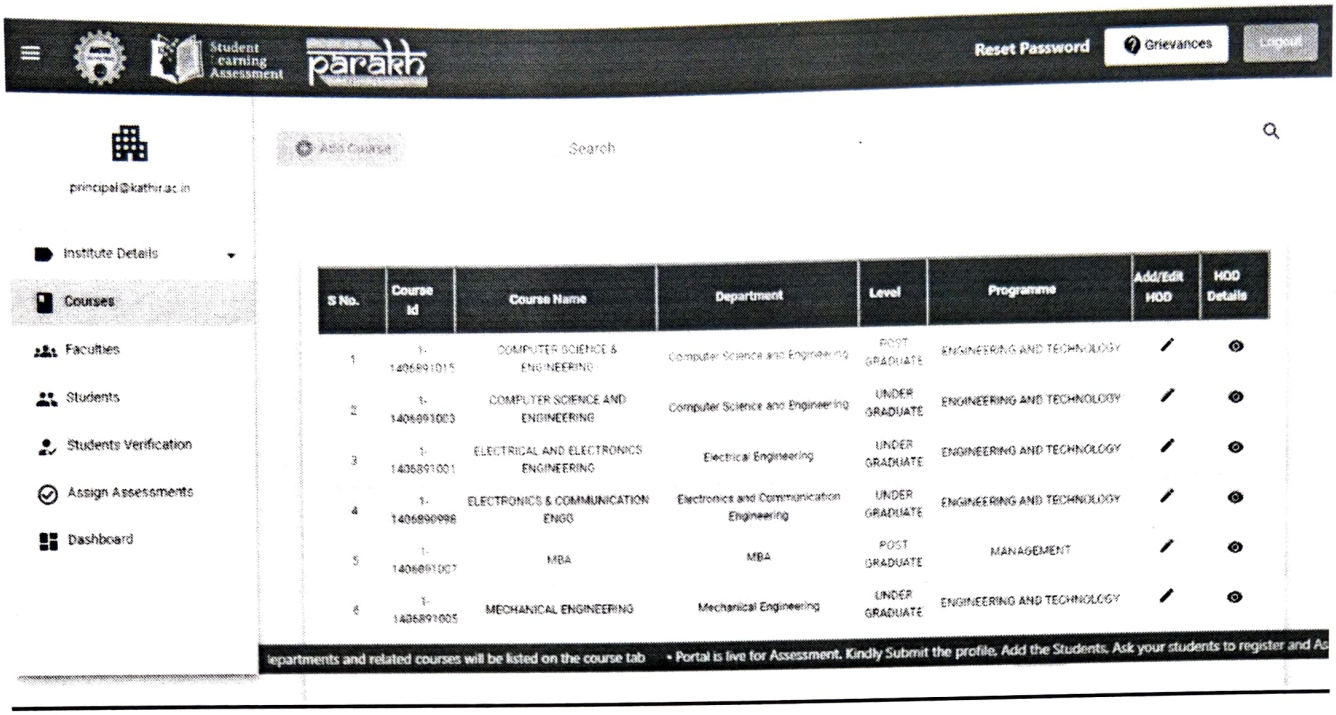
Neelambur,Coimbatore - 641 06



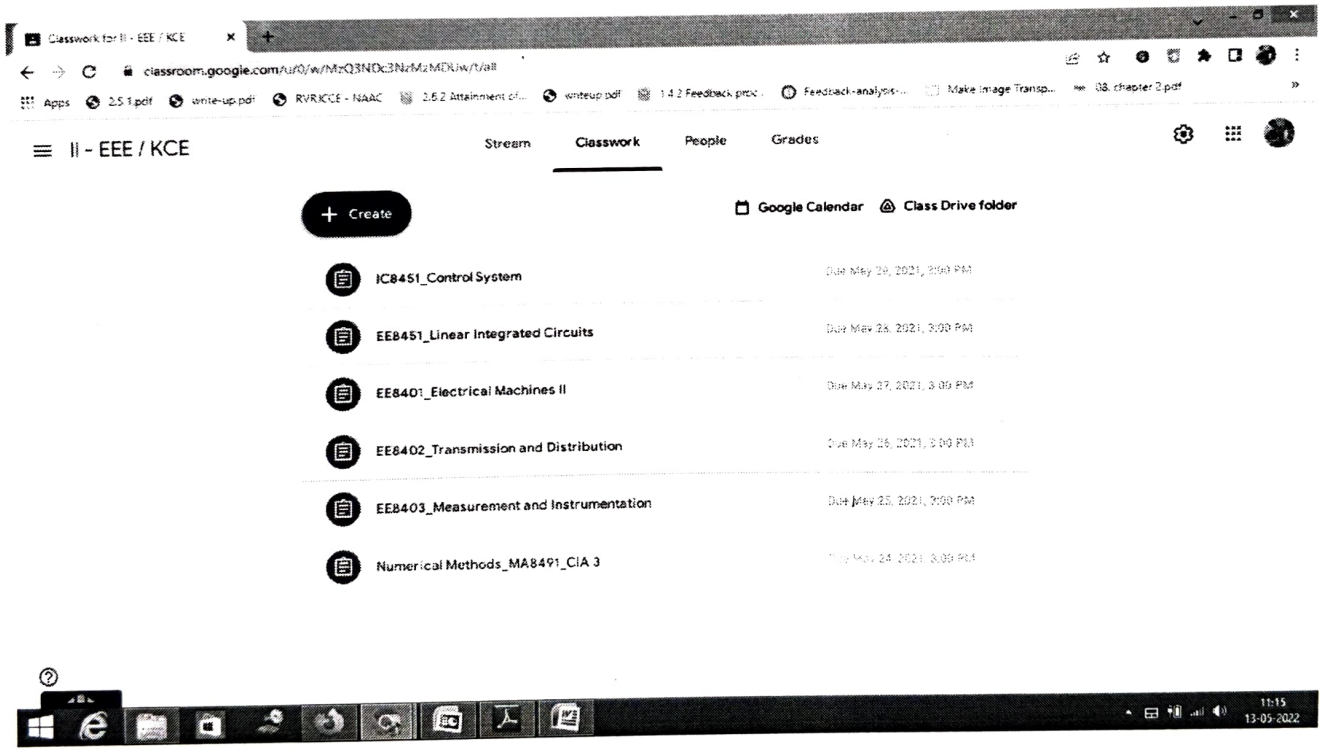
AICTE – PARAKH FOR TEACHING AND LEARNING







Usage of Google Classroom



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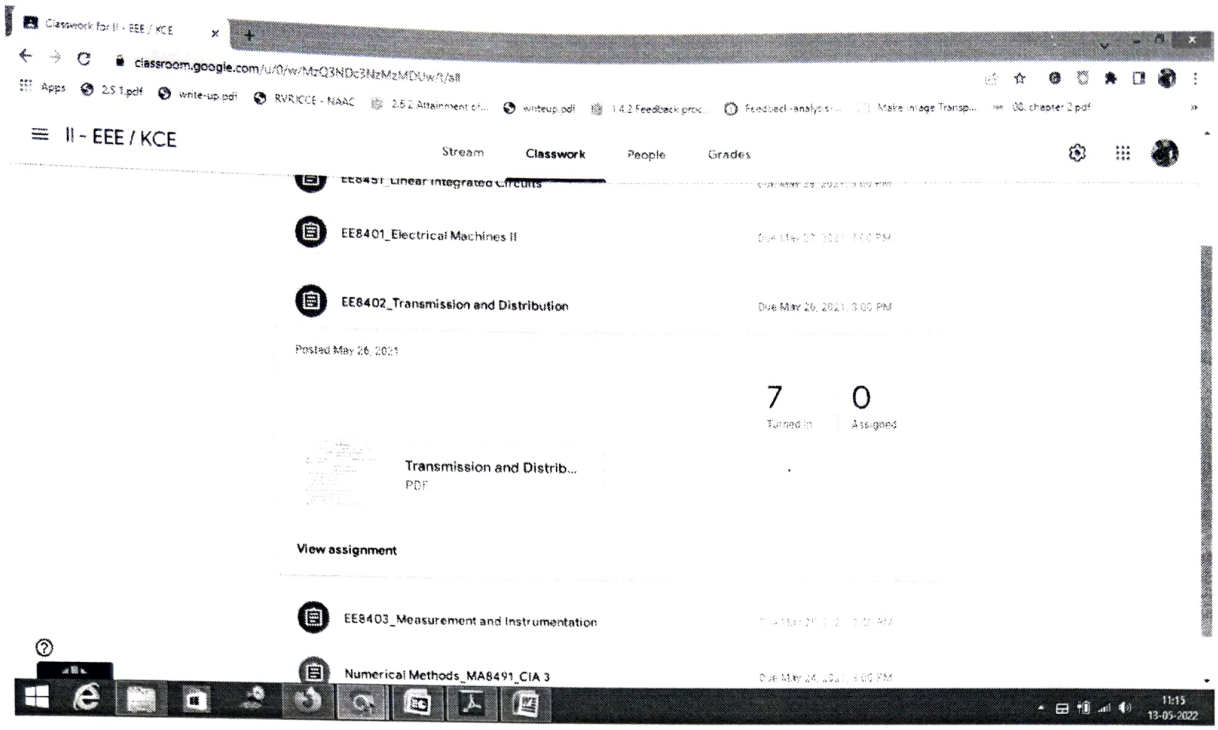

Virtual Labs for Teaching and Learning with NITK Surathkal

Virtual Labs

CERTIFICATE OF RECOGNITION

It is hereby certified that

Kathir College of Engineering

has been an active Nodal Centre of Virtual Labs under the National Mission on Education through Information and Communication Technology during the period

from **02-03-2022** to **31-12-2022**

with National Institute of Technology Karnataka (NITK), Surathkal as the mentor Participating Institute.

We look forward to your active collaboration along the road ahead for this novel initiative.

Dr. K. V. Gangadharan
Participating Institute Coordinator
Virtual Labs Project
NITK Surathkal.

Dr. Sheena
Institute Outreach Coordinator
Virtual Labs Project
NITK Surathkal.

PARTICIPATING INSTITUTES

Evolve with CSD

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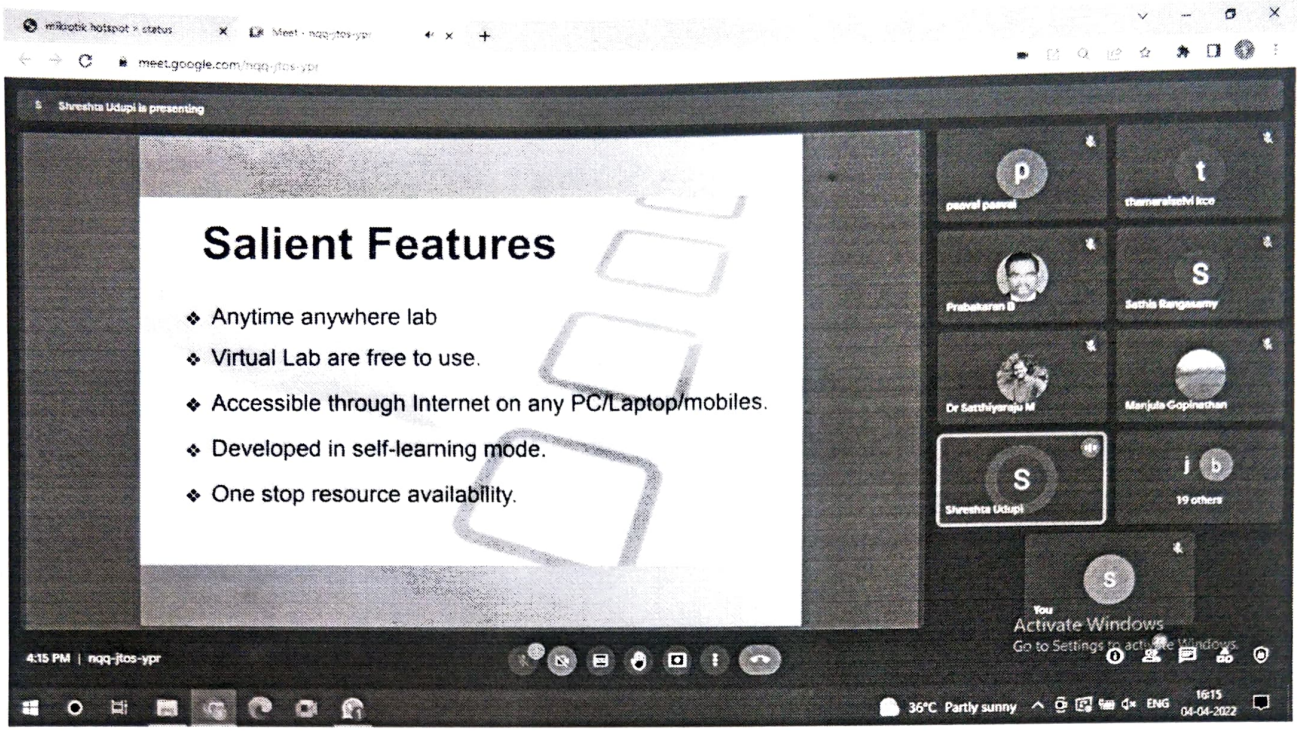

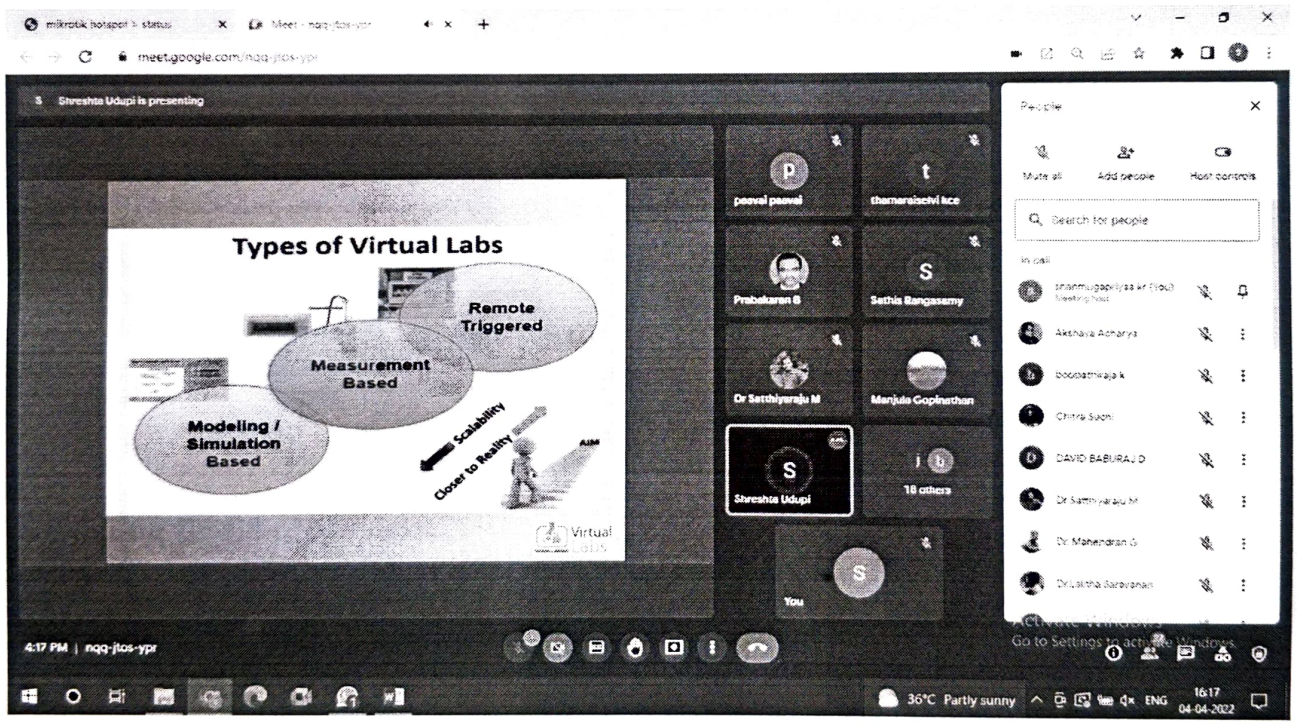

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