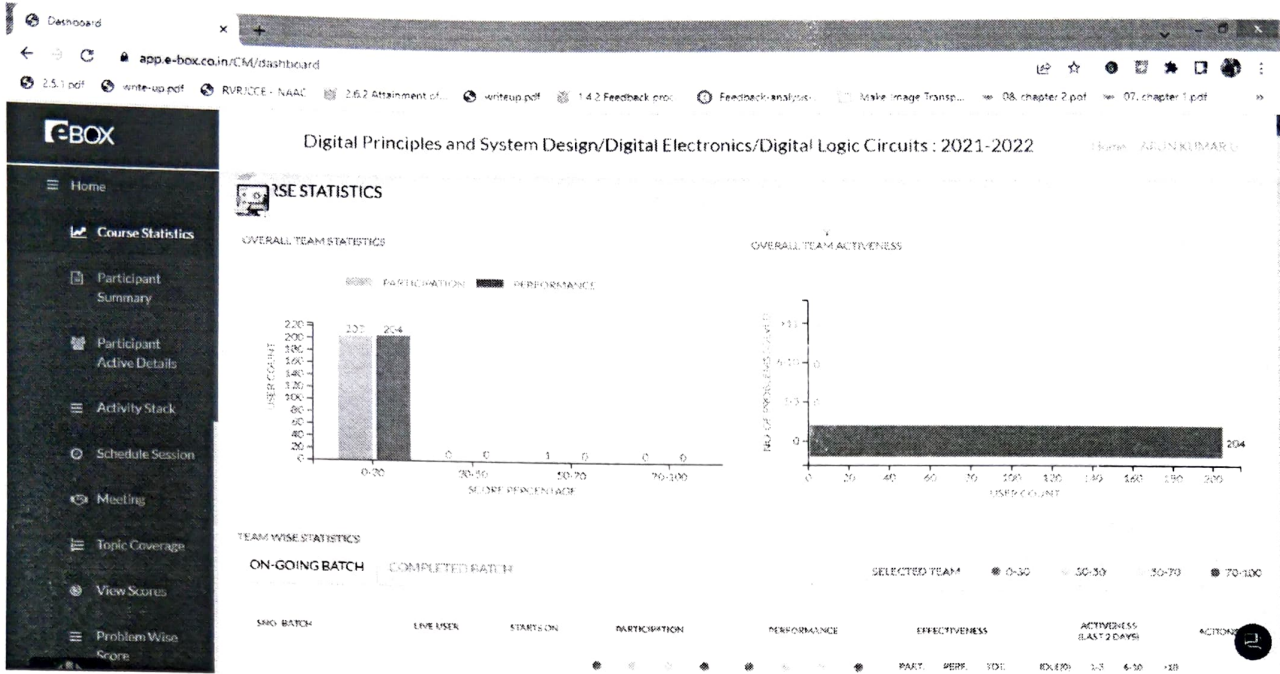


# Examination –ScreenShot of Tech Enabled Assessment:



**ATTENDANCE REPORT USING SESSION ATTEMPT**

Module	Session	Team	Status
Introduction and review of Numb...	Number Systems, Arithmetic O...	KCE_2024_CSE	Current Status

Search

SNO	REGISTER NUMBER	NAME	ATTENDANCE
1	KCE20C5001	Anu Surya N	Present
2	KCE20C5003	Deepak R	Present
3	KCE20C5004	Dharshini T	Present
4	KCE20C5005	DARSHINI PRABHA R	Present
5	KCE20C5006	Dhivyadharshini M	Present
6	KCE20C5008	John Prabhu G	Present
7	KCE20C5009	Karthikeyan J	Present



*Dr. R. UDAYAKUMAR, ME., Ph.D.,*  
 Principal  
 Kathir College of Engineering  
 "Wisdom Tree" Avinashi Road,  
 Neelambur, Coimbatore - 641 062.

Dashboard

app.e-box.co.in/CM/dashboard

2.5.1.pdf write-up.pdf RVR/KCE - NAAC 2.6.2 Attainment of... write-up.pdf 1.4.2 Feedback proc... Feedback analysis... Make image Transp... 08 chapter 2.pdf 07 chapter 1.pdf

### Digital Principles and System Design/Digital Electronics/Digital Logic Circuits : 2021-2022

Participant: ARUNKUMAR

S.No	Session	Module	Start Time	End Time	Participant	Score
1	Lecture Session XV	DPSD/DE/DLC 2021-22	18-10-2021 11:00	18-10-2021 12:30	arun.udayakumarn@gmail.com	55
5	Lecture Session XIV	DPSD/DE/DLC 2021-22	11-10-2021 11:00	11-10-2021 12:30	arun.udayakumarn@gmail.com	47
6	Lecture Session XIII	DPSD/DE/DLC 2021-22	07-10-2021 11:00	07-10-2021 12:30	arun.udayakumarn@gmail.com	48
7	Lecture Session XII	DPSD/DE/DLC 2021-22	30-09-2021 11:00	30-09-2021 12:30	arun.udayakumarn@gmail.com	46
8	Lecture Session XI	DPSD/DE/DLC 2021-22	27-09-2021 11:00	27-09-2021 12:30	arun.udayakumarn@gmail.com	28
9	Lecture Session X	DPSD/DE/DLC 2021-22	23-09-2021 11:00	23-09-2021 12:30	arun.udayakumarn@gmail.com	23
10	Lecture Session IX	DPSD/DE/DLC 2021-22	20-09-2021 11:00	20-09-2021 12:30	arun.udayakumarn@gmail.com	25
11	Lecture Session VIII	DPSD/DE/DLC 2021-22	16-09-2021 11:00	16-09-2021 12:30	arun.udayakumarn@gmail.com	23
12	Lecture Session VII	DPSD/DE/DLC 2021-22	13-09-2021 11:00	13-09-2021 12:30	arun.udayakumarn@gmail.com	23
13	Lecture Session VI	DPSD/DE/DLC 2021-22	09-09-2021 11:00	09-09-2021 12:30	arun.udayakumarn@gmail.com	23
14	Lecture Session V	DPSD/DE/DLC 2021-22	06-09-2021 11:00	06-09-2021 12:30	arun.udayakumarn@gmail.com	25
15	Lecture session IV	DPSD/DE/DLC 2021-22	02-09-2021 11:00	02-09-2021 12:30	arun.udayakumarn@gmail.com	18
16	Lecture Session III	DE/DLC/DPSD 2021	26-08-2021 11:00	26-08-2021 12:30	arun.udayakumarn@gmail.com	19
17	Introduction to Digital Logic Design	Lecture Session	19-08-2021 10:40	19-08-2021 12:15	arun.udayakumarn@gmail.com	22

Dashboard

app.e-box.co.in/CM/dashboard

2.5.1.pdf write-up.pdf RVR/KCE - NAAC 2.6.2 Attainment of... write-up.pdf 1.4.2 Feedback proc... Feedback analysis... Make image Transp... 08 chapter 2.pdf 07 chapter 1.pdf

### Digital Principles and System Design/Digital Electronics/Digital Logic Circuits : 2021-2022

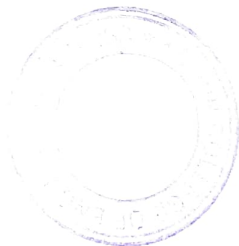
Participant: ARUNKUMAR

#### TICE / ASSESSMENT SCORE DETAILS

Module	Session	Grade Component	Team
Introduction and review of Num...	Number Systems, Arithmetic O...	-Select Grade Component-	KCE_2024_CSE

Search:

S.NO	REGISTER NUMBER	NAME	STATUS	SCORE (%)	GRACE TIME	START TIME	END TIME	CI	REMARK
1	KCE20CS017	Sri Sakthi M	Pass	80.0 %		05-09-2021 10:55		80.0	Pass
2	KCE20CSE702	Jalsurhan S	Pass	70.0 %		07-10-2021 15:46		70.0	Pass
3	KCE20CS015	Rithika M S	Pass	70.0 %		02-09-2021 23:52		70.0	Pass
4	KCE20CS011	Manohar Sah	Pass	70.0 %		25-08-2021 19:35		70.0	Pass
5	KCE20CS005	DARSHINI PRABHAR	Pass	60.0 %		26-08-2021 14:13		60.0	Pass
6	KCE20CS020	Naveen Kumar N	Pass	60.0 %		10-09-2021 14:16		60.0	Pass



*AR*

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"Wildern Tree" Avinashi Road,  
Neelambur, Coimbatore - 641 062.



Sri Sakthi M

KCE20CS017

Kathir College of Engineering

Outliers



**1/28**  
BATCH RANK

**71**  
TOTAL HOURS SPENT

**7/53**  
TOPICS COMPLETED

**0/56**  
SKILL PROBLEMS

**3024/1398**  
KNOWLEDGE PROGRAMS

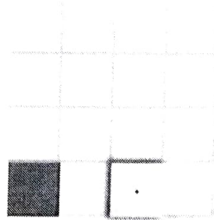
## Participation



**65%**

Attended 178 of 199 Sessions

## Quadrant Summary



QUADRANT 14

Low Calibre, Consistent Learner

**OUTLIERS**

### SUITABILITY

You are qualified for job roles offering 3L+ Salary.

### AIM FOR:

You can aim to become part of the Standard+ Group (4L+ salary)..

### HOW TO IMPROVE YOUR METRICS?

- 1) Have confidence in your abilities and avoid solving problems as a group.
- 2) Solve them individually. Attend all nugget assessments to improve your confidence level.
- 3) Rework on the topics/exercises in which you lack confidence by which your completion will improve.

## Performance

**0%**


Attended 2 of 54 Assessments

## Practice Session Score Details

SNO	TOPIC	I-LEARN	I-EXPLORE	I-ANALYSE	I-DESIGN
1	Introduction and review of Number systems, Arithmetic operations and Binary Codes	100.0%	80.0%	0.0%	AB
2	Boolean Algebra and Logic Gates - Theorems and Properties - I	100.0%	0.0%	AB	AB
3	Boolean Algebra and Logic Gates - Theorems and Properties - II	100.0%	0.0%	0.0%	AB
4	Boolean Functions - Canonical and Standard Forms - I	100.0%	0.0%	AB	AB
5	Boolean Functions - Canonical and Standard Forms - II	100.0%	20.0%	AB	AB
6	Simplification of Boolean Functions using Karnaugh Map - I	100.0%	80.0%	13.33%	68.75%
7	Simplification of Boolean Functions using Karnaugh Map - II	100.0%	100.0%	48.67%	81.25%
8	Simplification of Boolean Functions using Karnaugh Map - III	100.0%	100.0%	100.0%	80.42%
9	Simplification of Boolean Functions using Karnaugh Map - Example Problems - 1	100.0%	80.0%	100.0%	93.75%
10	Simplification of Boolean Functions using Karnaugh Map - Example Problems - 2	100.0%	100.0%	48.67%	81.25%
11	NAND and NOR Implementation	100.0%	100.0%	100.0%	68.75%
12	NAND and NOR Implementation - Example Problems	100.0%	100.0%	100.0%	50.0%
13	Combinational Circuits - Analysis and Design Procedures	100.0%	20.0%	AB	AB
14	Combinational Circuit Design - Example Problems - 1	100.0%	100.0%	50.0%	12.5%
15	Combinational Circuit Design - Example Problems - 2	100.0%	75.0%	50.0%	8.75%

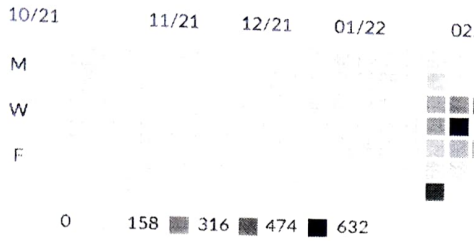
DR. R. UDAYAKUMAR, M.E., Ph.D.,  
Principal  
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"Wid in Tree" Avinashi Road,  
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16	Binary Adder-Subtractor -Decimal Adder-Binary Multiplier	100.0%	0.0%	0.0%	AB
17	Magnitude Comparator-Code converter	100.0%	100.0%	No Session	31.25%
18	Code Converters - Example Problems	100.0%	No Session	25.0%	0.0%
19	Decoder and Encoder	100.0%	100.0%	80.0%	12.5%
20	Multiplexer and Demultiplexer	80.0%	100.0%	100.0%	10.0%
21	MUX and DeMUX - Example Problems	100.0%	100.0%	100.0%	No Session
22	Logical Circuit Design - Example Problems	100.0%	100.0%	100.0%	0.0%
23	Introduction to HDL and HDL Models of Combinational circuits	AB	AB	AB	AB
24	Combinational and Logical Circuit Design - Example Programs	0.0%	0.0%	0.0%	0.0%
25	Sequential Circuits - SR,JK, T and D Flipflops and Latches. Types of Triggering	100.0%	2.38%	0.0%	0.0%
26	Analysis of Clocked Sequential Circuits	100.0%	0.0%	100.0%	0.0%
27	Flipflops, Sequential Circuit Analysis and Design - Example Problems - 1	100.0%	100.0%	100.0%	12.5%
28	Sequential Circuit Analysis and Design - Example Problems - 2	100.0%	100.0%	100.0%	No Session
29	State diagram, Reduction and Assignment	100.0%	100.0%	100.0%	No Session
30	State Reduction and Assignment - Example Problems	100.0%	100.0%	100.0%	No Session
31	Synchronous and Asynchronous Counters - Design Procedure	100.0%	40.0%	100.0%	25.0%
32	Synchronous and Asynchronous Counters - Example Problems and Shift Registers	100.0%	40.0%	100.0%	15.0%
33	Counters - Example Problems - 1	100.0%	20.0%	100.0%	23.33%
34	Counters and Shift Registers - Example Problems - 2	100.0%	20.0%	100.0%	8.33%
35	HDL Models of Sequential circuits	100.0%	100.0%	No Session	0.0%
36	Sequential Circuit Design - Example Programs	100.0%	100.0%	No Session	0.0%
37	Asynchronous sequential logic circuits-Transition stability, flow stability, PFT	100.0%	100.0%	33.33%	12.5% <span style="border: 1px solid black; padding: 2px;">2/2</span>
38	Analysis of asynchronous sequential logic circuits - I	100.0%	100.0%	10.0%	25.0%
39	Analysis of asynchronous sequential logic circuits - II	100.0%	100.0%	No Session	12.5%
40	Asynchronous sequential Circuit Analysis and Design - Example Problems - 1	100.0%	100.0%	No Session	16.67%
41	Flow diagram and Table - Reduction and Assignment	100.0%	100.0%	25.0%	0.0%
42	Flow diagram and Table - Reduction and Assignment - Example Problems	100.0%	100.0%	No Session	72.73%
43	Races, Cycles and Hazards	100.0%	100.0%	100.0%	No Session
44	Races, Cycles and Hazards - Example Problems	100.0%	100.0%	100.0%	No Session
45	RAM -Memory Decoding	100.0%	100.0%	0.0%	95.19%
46	Error Detection and Correction -ROM	100.0%	100.0%	82.5%	100.0%
47	Programmable Logic Array	100.0%	40.0%	0.0%	0.0%
48	Programmable Array Logic	100.0%	100.0%	No Session	100.0%
49	Digital Logic Families	100.0%	100.0%	100.0%	100.0%
50	Test	AB <span style="border: 1px solid black; padding: 2px;">0/2</span>	AB	AB	AB <span style="border: 1px solid black; padding: 2px;">0/2</span>

  
 Dr. R. UDAYAKUMAR, M.E., Ph.D.,  
 Associate Professor  
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### Problem Solved Metrics



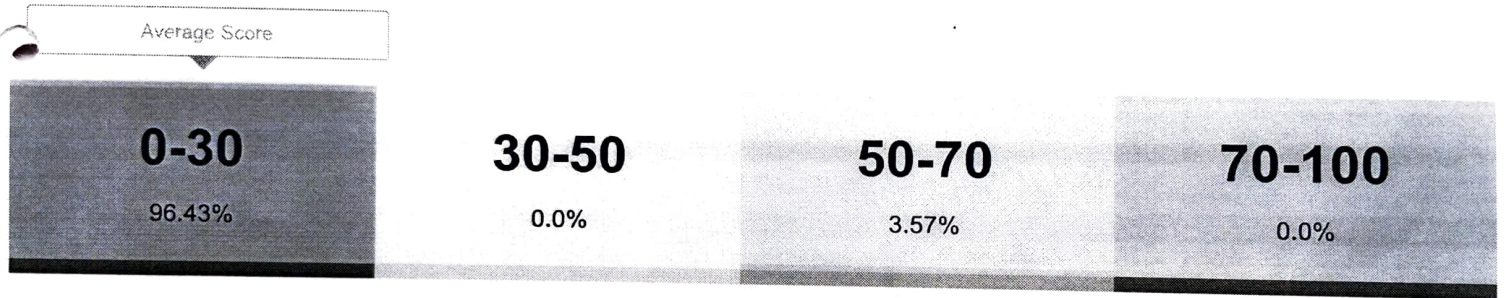
### Time Spent Metrics

Total Hour Spent:	71 Hrs
Total Day Spent:	34 Days
Average Time Spent:	2 Hrs

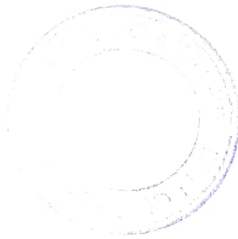
### Assessment Score Details

SNO	TOPIC	SESSION	ASSESSMENT DATE	SCORE
1	Error Detection and Correction -ROM	Error Detection and Correction -ROM	16-02-2022 03:02 PM	0.0
2	Programmable Array Logic	Programmable Array Logic	24-02-2022 11:02 AM	0.0

### User Score Status



Sri Sakthi M



*[Handwritten Signature]*  
 Lecturer in Charge  
 "Widened Horizons" Engineering  
 Neelanbar, Coimbatore - 641 062.

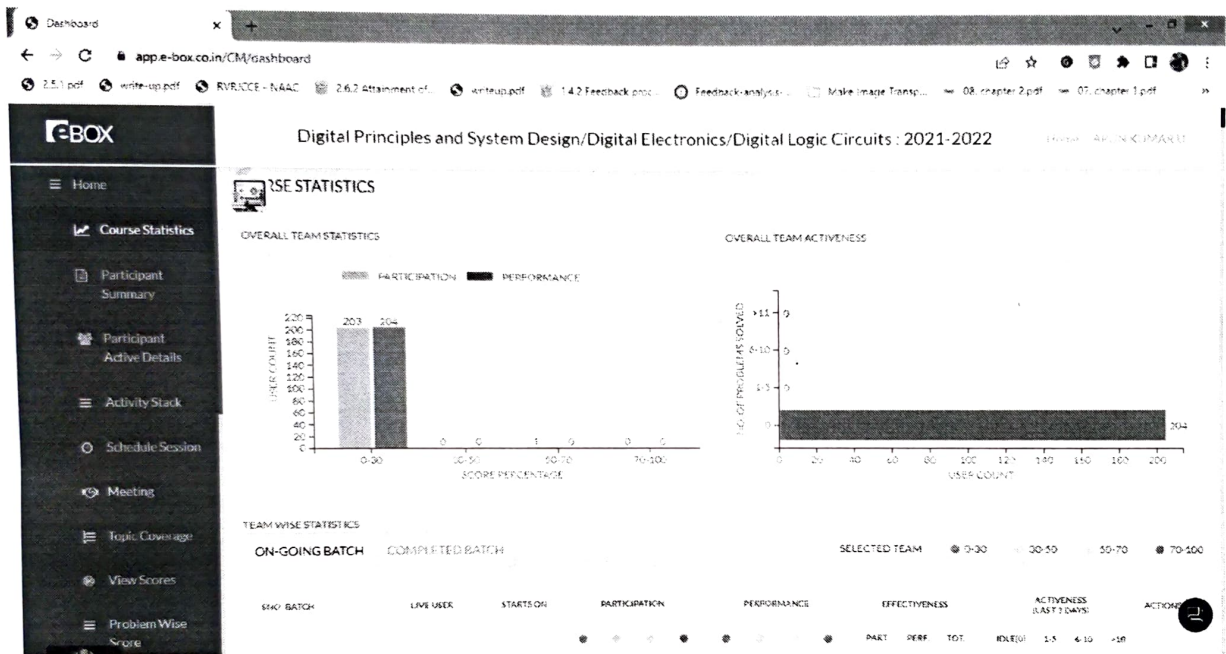


# Kathir College of Engineering

[Approved by AICTE | Affiliated to Anna University | Accredited by NAAC]  
 Wisdom Tree, Neelambur, Avinashi Road, Coimbatore-62

## Activities Implemented Based on Strategic Planning

### Following Effective Teaching – Learning Process (Tech Enabled Teaching and Learning)



**Digital Principles and System Design/Digital Electronics/Digital Logic Circuits : 2021-2022**

**ATTENDANCE REPORT USING SESSION ATTEMPT**

Module	Session	Team	Status
Introduction and review of Numb...	Number Systems, Arithmetic O...	KCE_2024_CSE	Current Status

Search

SNO	REGISTER NUMBER	NAME	ATTENDANCE	
<input type="checkbox"/>	1	KCE20CS001	Anu Surya N	Present
<input type="checkbox"/>	2	KCE20CS003	Deepak P	Present
<input type="checkbox"/>	3	KCE20CS004	Dharshini T	Present
<input type="checkbox"/>	4	KCE20CS005	DIARSHINI PRABHA R	Present
<input type="checkbox"/>	5	KCE20CS006	Dhivyadharshini M	Present
<input type="checkbox"/>	6	KCE20CS008	John Prabhu G	Present
<input type="checkbox"/>	7	KCE20CS007	Karthikeyan J	Present

Dr. R. UDAYAKUMAR, M.E., Ph.D.,  
 Principal  
 Kathir College of Engineering  
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 Neelambur, Coimbatore - 641 062.

Dashboard

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Digital Principles and System Design/Digital Electronics/Digital Logic Circuits - 2021-2022

Sl. No	Topic	Start Date	End Date	Score	Grade
1	Lecture 1: Introduction to Digital Logic	21-09-2021	27-09-2021	85.00	A
2	Lecture 2: Boolean Algebra	28-09-2021	04-10-2021	78.00	B
3	Lecture 3: Combinational Logic	05-10-2021	11-10-2021	92.00	A
4	Lecture 4: Sequential Logic	12-10-2021	18-10-2021	88.00	B
5	Lecture 5: Timing Diagrams	19-10-2021	25-10-2021	75.00	C
6	Lecture 6: Digital Multiplexers and Demultiplexers	26-10-2021	01-11-2021	80.00	B
7	Lecture 7: Digital Decoders and Encoders	02-11-2021	08-11-2021	72.00	C
8	Lecture 8: Digital Adders and Subtractors	09-11-2021	15-11-2021	85.00	A
9	Lecture 9: Digital Comparators	16-11-2021	22-11-2021	78.00	B
10	Lecture 10: Digital Counters	23-11-2021	29-11-2021	82.00	B
11	Lecture 11: Digital Shift Registers	30-11-2021	06-12-2021	75.00	C
12	Lecture 12: Digital Memory Elements	07-12-2021	13-12-2021	88.00	B
13	Lecture 13: Digital Memory Structures	14-12-2021	20-12-2021	80.00	B
14	Lecture 14: Digital Bus Structures	21-12-2021	27-12-2021	72.00	C
15	Lecture 15: Digital Interfacing	28-12-2021	03-01-2022	85.00	A
16	Lecture 16: Digital Signal Processing	04-01-2022	10-01-2022	78.00	B
17	Final Examination	11-01-2022	17-01-2022	82.00	B

Dashboard

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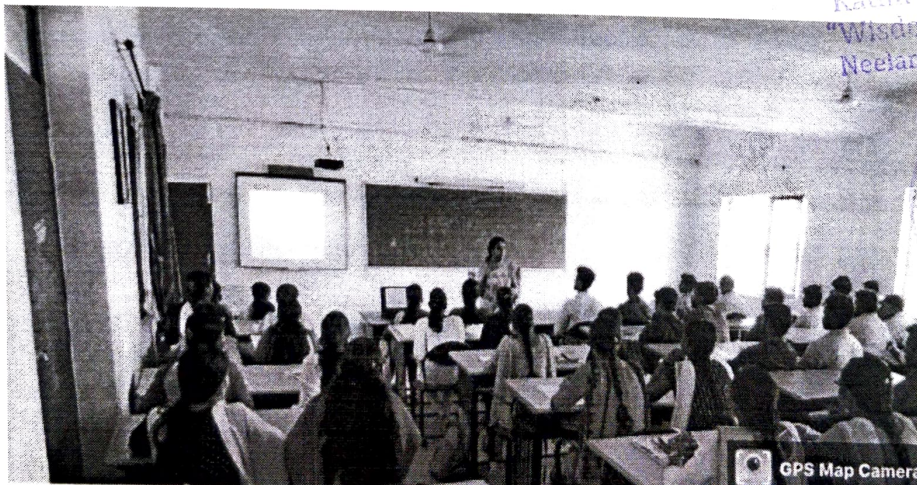
Digital Principles and System Design/Digital Electronics/Digital Logic Circuits - 2021-2022

GRADE / ASSESSMENT SCORE DETAILS

Sl. No	Module	Session	Grade	Component	Score	Grade
1	Introduction and review of Names	Number Systems, Arithmetic	A	Number Systems Component	85.00	A
2	Boolean Algebra	Boolean Algebra	B	Boolean Algebra Component	78.00	B
3	Combinational Logic	Combinational Logic	A	Combinational Logic Component	92.00	A
4	Sequential Logic	Sequential Logic	B	Sequential Logic Component	88.00	B
5	Digital Multiplexers and Demultiplexers	Digital Multiplexers and Demultiplexers	C	Digital Multiplexers and Demultiplexers Component	75.00	C
6	Digital Decoders and Encoders	Digital Decoders and Encoders	B	Digital Decoders and Encoders Component	80.00	B
7	Digital Adders and Subtractors	Digital Adders and Subtractors	A	Digital Adders and Subtractors Component	85.00	A
8	Digital Comparators	Digital Comparators	B	Digital Comparators Component	78.00	B
9	Digital Counters	Digital Counters	C	Digital Counters Component	72.00	C
10	Digital Shift Registers	Digital Shift Registers	A	Digital Shift Registers Component	85.00	A
11	Digital Memory Elements	Digital Memory Elements	B	Digital Memory Elements Component	88.00	B
12	Digital Memory Structures	Digital Memory Structures	C	Digital Memory Structures Component	75.00	C
13	Digital Bus Structures	Digital Bus Structures	B	Digital Bus Structures Component	80.00	B
14	Digital Interfacing	Digital Interfacing	A	Digital Interfacing Component	85.00	A
15	Digital Signal Processing	Digital Signal Processing	B	Digital Signal Processing Component	78.00	B
16	Final Examination	Final Examination	C	Final Examination Component	72.00	C

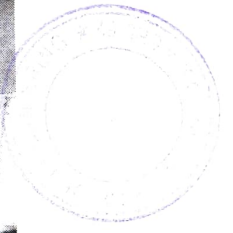
**Following Effective Teaching – Learning Process (Smart Board Usage)**

*Dr. R. UDAYAKUMAR, ME., Ph.D.*  
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Kathir College  
of Engineering  
Google

**Neelambur, Tamil Nadu, India**  
Main Block, Way to Kathir College Main Block, Neelambur,  
Tamil Nadu 641062, India  
Lat 11.06801°  
Long 77.083055°  
03/25/22



GPS Map Camera



*Handwritten signature and a green arrow pointing towards the top right.*

*UDAIYANUMAR, ME., Ph.D.,  
Principal  
Kathir College of Engineering  
"Wisdoin Tree" Avinashi Road,  
Neelambur, Coimbatore - 641 062.*

## AICTE – PARAKH FOR TEACHING AND LEARNING

**Dashboard**

- Total Assessment: 0 (0% from last Week)
- Student Assessments: 0 (Out of 338 Students)
- Avg. Score Student: N/A (0% from last Week)
- Rank: 1451 (Out of 582 Institutions)

Dashboard of KATHIR COLLEGE OF ENGINEERING

Department: [Dropdown]

Student Assessment Count - Monthwise

Assessments by Institute: [Bar Chart showing 1.4]

Top Disciplines: No Data

\* Assessments can be carried out Civil, Mechanical, Electrical, Electronics & Comm.

**Student Gap Analysis**

Not Registered	Not Registered	Profile Not Submitted	Verification Pending	Assessment Not Ass.	Assessment Not Tak.
178	215	207	0	184	0

Student Assessments ( Not Registered )

Search in Not Registered Students [Search Icon] [Export Data]

Student Id	Name	Discipline	Batch	Current Year	Contact Info
SLAS46047	DHEENATHAYALAN	ELECTRONICS AND COMMUNICATION ENGINEERING	2019	0	[Phone Icon]
SLAS46052	JAYARAM L	ELECTRONICS AND COMMUNICATION ENGINEERING	2019	0	[Phone Icon]

\* Assessments can be carried out Civil, Mechanical, Electrical, Elect



Student Learning Assessment **parakth** Reset Password Grievances Logout

principal@kathir.ac.in

**Institute Details**

**Courses**

Faculties

Students

Students Verification

Assign Assessments

Dashboard

S No.	Course Id	Course Name	Department	Level	Programme	Add/Edit HOD	HOD Details
1	1-1406891015	COMPUTER SCIENCE & ENGINEERING	Computer Science and Engineering	POST GRADUATE	ENGINEERING AND TECHNOLOGY		
2	1-1406891003	COMPUTER SCIENCE AND ENGINEERING	Computer Science and Engineering	UNDER GRADUATE	ENGINEERING AND TECHNOLOGY		
3	1-1406891001	ELECTRICAL AND ELECTRONICS ENGINEERING	Electrical Engineering	UNDER GRADUATE	ENGINEERING AND TECHNOLOGY		
4	1-1406890998	ELECTRONICS & COMMUNICATION ENGG	Electronics and Communication Engineering	UNDER GRADUATE	ENGINEERING AND TECHNOLOGY		
5	1-1406891007	MBA	MBA	POST GRADUATE	MANAGEMENT		
6	1-1406891005	MECHANICAL ENGINEERING	Mechanical Engineering	UNDER GRADUATE	ENGINEERING AND TECHNOLOGY		

Departments and related courses will be listed on the course tab - Portal is live for Assessment. Kindly Submit the profile. Add the Students, Ask your students to register and As

## Usage of Google Classroom

Classwork for II - EEE / KCE

classroom.google.com/Au0/w/MzQ3NDc3NmZMDkxw/vall

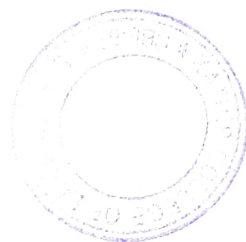
Apps 2.5.1.pdf write-up.pdf RVRKCE - NAAC 2.5.2 Attainment of... writeup.pdf 1.4.2 Feedback proc... Feedback analysis... Make Image Transp... US chapter 2.pdf

Stream **Classwork** People Grades

+ Create Google Calendar Class Drive folder

- IC8451\_Control System Due May 29, 2021, 3:59 PM
- EE8451\_Linear Integrated Circuits Due May 28, 2021, 3:59 PM
- EE8401\_Electrical Machines II Due May 27, 2021, 3:05 PM
- EE8402\_Transmission and Distribution Due May 26, 2021, 3:00 PM
- EE8403\_Measurement and Instrumentation Due May 25, 2021, 3:00 PM
- Numerical Methods\_MA8491\_CIA 3 Due May 24, 2021, 3:00 PM

Windows taskbar: 11:15 13-05-2022



*UD*

**Dr. R. UDAIYAKUMAR, ME., Ph.D.,**  
 Principal  
 Kathir College of Engineering  
 "Wisdom Tree" Avinashi Road,  
 Neelambur, Coimbatore - 641 062.



Shreshtha Udipi is presenting

# Salient Features

- ❖ Anytime anywhere lab
- ❖ Virtual Lab are free to use.
- ❖ Accessible through Internet on any PC/Laptop/mobiles.
- ❖ Developed in self-learning mode.
- ❖ One stop resource availability.

4:15 PM | nqq-jtos-ypr

36°C Partly sunny

16:15  
04-04-2022

Shreshtha Udipi is presenting

# Types of Virtual Labs

4:17 PM | nqq-jtos-ypr

36°C Partly sunny

16:17  
04-04-2022

Dr. R. UDAYAKUMAR, ME., Ph.D.,  
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